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A Novel of PSO Modified Carrier-Based PWM Technique to Reduce Total Harmonic Distortion in The Inverter Topology 7-level Cascade H-Bridge Triple Voltage Boosting Gain

Moh. Zainul Falah, Sujito, Aripriharta
Department of Electrical and Inforamtics Engineering, State University of Malang, Malang, Indonesia

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ABSTRACT

This research focuses on optimizing the Particle Swarm Optimization (PSO) method in switching modulation to reduce total harmonic distortion (THD) in a 7-level Cascade H-Bridge Multi-Level Inverter (MLI) topology with triple voltage boosting gain. MLI Cascade H-Bridge is an inverter topology that is widely used in power conversion applications because of its ability to produce high voltage output with low harmonics. However, the resulting THD is still a major challenge in improving power quality. In this research, the PSO method is applied to find optimal parameters in switching modulation that can minimize THD. The research results show that the PSO method succeeded in reducing THD significantly with a THD value of 7.80% whereas the previous THD was 17.27%. The implementation of PSO in switching modulation is expected to be an effective solution for inverter applications in industry and power systems. The THD value from the PSO optimization is stated to be in accordance with IEEE 519 standards with a maximum permitted THD of 8%. This value is better than previous research, namely 17.27%.

Corresponding Author:

Sujito, Department of Electrical and Informatics Engineering, State University of Malang, Malang 65151, Indonesia
Email: sujito.ft@um.ac.id

1. INTRODUCTION

Nowadays, multilevel inverters (MLI) play a major role in various power quality applications such as Electric Vehicles [1], photovoltaic systems [2], Low-Power Loads [3], and integrated grid systems [4]. This is important because it is associated with lower values of harmonic distortion and switching losses [5], [6], [7].

In current developments, the use of multilevel inverter (MLI) topology has developed rapidly in the field of power electronics and has various promising applications for more advanced technology. MLI has high power quality and can produce an output voltage with a wave shape resembling a ladder with levels according to the number of MLI levels [8]. There are several types of MLI topologies known, such as NPC, flying capacitors or clamped capacitors, diode clamped, and cascaded H-bridge (CHB) [9], [10], [11], [12]. However, each topology has certain disadvantages. To overcome this problem, a new topology was implemented which combines the CHB topology and flying capacitors topology. This new topology is suitable for overcoming the problems of the number of components and switching used and has a seven-level output waveform [13], [14], [15], [16]. MLI implementations that exceed seven levels require a more complicated number of components and switching arrangements, while MLI implementations that do not reach 15 levels result in poor THD. The CHB topology has a higher output with a rational increase in switching devices [17], [18], [19], [20], [21], while the capacitor can overcome the problem of unbalanced voltage and help increase the boosting gain at the output [22], [23], [24].

Multilevel inverter systems use Pulse Width Modulation (PWM) to control switching on MOSFETs [25], [26], [27], [28]. Various modulation techniques are used, including Selective Harmonic Elimination PWM

(SHEPWM), Sine PWM (SPWM), Space Vector PWM (SVPWM), and similar variations [29], [30]. SPWM is the most popular technique because it reduces harmonics by manipulating the carrier signal, has low switching advantages, and is easy to implement [30], [31]. However, SPWM still produces quite high harmonic distortion in single-phase inverters. In this research, the POD (Phase Opposition Disposition) type SPWM modulation technique was used because it has a better THD value than other modulation techniques such as PD (Phase Disposition) and APOD (Alternative Opposition Disposition) [32]. However, in previous research, the MLI topology with SPWM modulation techniques still produced a high THD, namely 17.27% [33]. Therefore, carrier signal optimization is carried out to reduce the THD value. THD limit values and power quality standards as specified in IEEE recommendation 519 [34] to limit the magnitude of harmonics to 8% of the fundamental component.

The PSO algorithm is a meta-heuristic algorithm that uses swarm intelligence to find the optimal solution to a problem [35], [36], [37]. PSO algorithms are a specific class of evolutionary algorithms that use techniques inspired by the social behavior of birds searching for food in specific areas. This is a simple algorithm. Basically, PSO is a global optimization technique, with optimization methods to obtain more accurate search capabilities. PSO starts the procedure with initialization and generating a random initial population. After evaluating each particle, the best local and global iteration positions are updated. The next step is to carry out iterations starting from the newly formed particles according to their initial position, initial velocity, and best local and global positions. The implementation of the PSO algorithm can be done by using initial initialization settings [38], [39], [40], [41]. This initial initialization value can be used as an estimate or prediction of the particle value in the next iteration. In PSO, the particle value in the next iteration is calculated by combining the particle value in the previous iteration and the best particle value in the entire population.

Based on these problems, this research was carried out. Previous research [13] In his research, the Total Harmonic Distortion produced was 17.27%, and researchers interested in making improvements started by modeling the topology. This topology only uses one DC source and two capacitors and the resulting output voltage gain is close to 3Vdc and is able to reduce voltage stress. The next stage is to apply the PSO-based SPWM modulation technique to regulate the on-off switch on the MOSFET based on the carrier signal with time value, frequency, and THD parameters.

2. METHODS

2.1. Design of Topology 7 level Inverter Cascade H- Bridge Triple Voltage Boosting Gain

In the block diagram, the research procedure in Fig. 1 begins by carrying out a 7-level Cascade H-Bridge Triple Boosting Gain Inverter Simulation with SPWM modulation techniques, to obtain optimization values for the carrier signal in reducing THD. The initial process is carried out with initialization. Next, the data obtained is processed using the PSO algorithm to produce the best Pbest and Gbest values with THD fitness values below 8% [42]. The expected THD standard is below 8%. Research procedures related to MLI can be seen in Fig. 1.

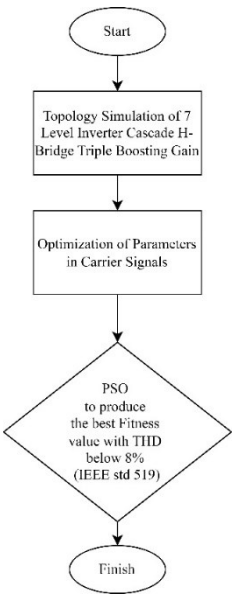

Fig. 1. Flowchart Research

2.2. MLI with SPWM

According to research conducted by [13], [43], In this research, a new topology is used which combines the 7-Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology as shown in Fig. 2. This topology consists of three CHB topologies, where the CHB topology in the middle is connected to a Direct Current voltage source. (DC), while the CHB topology at the front and rear is connected to a capacitor which acts as a floating capacitor topology. In this research, there were 16 MOSFETs and 2 capacitors used. There is a neutral terminal in the CHB topology shown in S5 and S10 connected to a component that functions as a two-way voltage blocker in the image Fig. 3. The two-way voltage blocking component is composed of two MOSFETs with the MOSFET source terminals connected together. The value of each component is shown in Table 1.

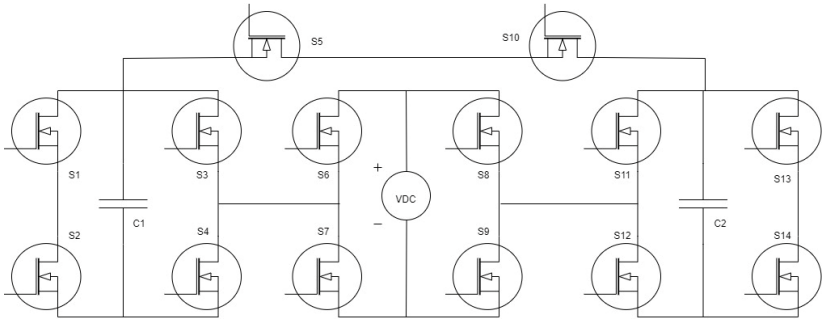

Fig. 2. Topology 7 Level Inverter Cascade H- Bridge Triple Voltage Boosting Gain

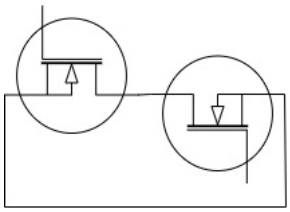

Fig. 3. Two-Way Voltage Blocking Switch

Table 1 Inverter Component

No	Component Type	Value	Total
1	Capasitor	4700 uF	2
2	MOSFET (N-Channel)	10 A, 1200 V	16
3	Input Voltage	30 V	1
4	R_L	500 ohm	1

Total Harmonic Distortion (THD) is the percentage value of the total current or voltage obtained by comparing the value of the harmonic components of the current or voltage to the current and voltage values at the basic frequency. THD is used to measure the extent to which a periodic waveform containing harmonics deviates from its ideal sinusoidal shape. The higher the THD percentage, the greater the risk of equipment damage. The THD value for the current and voltage waveforms is expressed in the following equation [44]:

$$THD_i = \sqrt{\frac{\sum_{h=2}^{\infty} I_h^2}{I_1}} x100\% \quad (1)$$

and

$$THD_v = \sqrt{\frac{\sum_{h=2}^{\infty} V_h^2}{V_1}} x100\% \quad (2)$$

THD_i is total harmonic distortion current (%), THD_v is total harmonic distortion voltage (%), I_h is harmonic currents of the h order (A), V_h is harmonic voltage of the h order (V), I_1 is current fundamental (A), V_h is voltage fundamental (V).

2.3. PSO (Particle Swarm Optimization)

PSO Method in Switching to Produce Sinusoidal Signals with a 7-Level Inverter Cascade H- Bridge Topology Triple Voltage Boosting Gain is a method and Particle Swarm Optimization (PSO) for producing sinusoidal signals with a 7 Level Inverter Cascade H-Bridge Topology Triple Voltage Boosting Gain.

Particle Swarm Optimization (PSO) works based on the collective behavior of particles moving through a multidimensional search space to find the optimal solution. This method is inspired by the social behavior of flocks of birds or schools of fish, where each particle adjusts its position and velocity according to its own experience and the experience of the particles around it. The main steps in the PSO process can be explained as follows:

- Initialization: The algorithm starts by initializing a population of particles with random positions and velocities in the search space.
- evaluation: Each particle position is evaluated based on a fitness function, which determines the quality of the solution at that position.
- updating Personal Best: Each particle compares the fitness value of its current position with its previous best position. If the current position provides better results, the personal best will be updated.
- updating Global Best: Additionally, each particle compares the fitness value of its current position with the best global position found by the entire group. If a better solution is found, the global best position will be updated.
- Velocity and Position update: Using cognitive and social components, each particle adjusts its velocity and position considering its personal best, global best, and momentum factors. This adjustment aims to direct the particles towards the optimal solution while avoiding premature convergence.
- Update Particle Velocity

$$V_i(t+1) = w.v_i(t) + c_1.r_i.\left(pbest_i - x_i(t)\right) + c_2.r_2.(gbest - x_i(t)) \quad (3)$$

$(t+1)$ is velocity of particle i at iteration $t+1$ $t+1$, w is inertia factor, $c_1 c_2$ is Acceleration coefficient, $r_i r_2$ is random number between 0 and 1, $pbest_i$ is the best position ever reached by particle i, (t) is position of particle i at iteration t, $gbest$ is the best position ever achieved by an entire population

- Update particle position

$$x_i(t+1) = x_i(t) + v_i\,(t+1) \quad (4)$$

$x_i(t+1)$ is position of particle i at iteration $t+1$, $x_i(t)$ is position of particle i at iteration t, $v_i\,(t+1)$ is velocity position of particle i at iteration $t+1$

- Termination Condition: The process continues iteratively until a certain termination condition is met, such as reaching a maximum number of iterations or achieving a desired level of solution accuracy.

By continuously updating their velocity and position based on their individual experience and shared knowledge of the swarm, the particles efficiently explore and exploit the search space, thereby leading to the identification of optimal or near-optimal solutions to complex optimization problems.

The PSO technique is a method used to improve the accuracy and velocity of the duty cycle setting process in the switching process in the 7 Level Inverter Cascade H-Bridge topology Triple Voltage Boosting Gain which will be used to optimize the parameter values required in the 7 Level Inverter Cascade H-Bridge topology Triple Voltage Boosting Gain, such as input voltage, number of MOSFETs, and PSO optimization parameters. This technique optimizes an objective function using a search process in a definable parameter space.

In the PSO method of Switching to Produce Sinusoidal Signals with a 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain Topology, the switching process in a 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology is regulated using the duty cycle produced by the PSO technique. The duty cycle is generated by predicting the optimal duty cycle value based on past data from sinusoidal signals and by reducing the effects of noise or fluctuations. Block diagram research shown in Fig. 4.

Next, the PSO technique is used to find the optimal values of the parameters required in the 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology, thereby producing an optimal sinusoidal signal. In this process, the PSO technique seeks optimal values of an objective function that describes the quality of the sinusoidal signal produced by the 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology (Fig. 5). MOSFET switching conditions shown in Table 2.

The PSO Switching Method for Generating Sinusoidal Signals with a 7 Level Cascade H-Bridge Triple Voltage Boosting Gain Inverter Topology has several advantages, such as:

a. Increasing the accuracy and velocity of the duty cycle setting process in the switching process in the 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology.
b. Optimizing the parameter values required in the 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology, thereby producing an optimal sinusoidal signal.
c. Can increase the efficiency of energy use, because it produces a better and more stable sinusoidal signal.

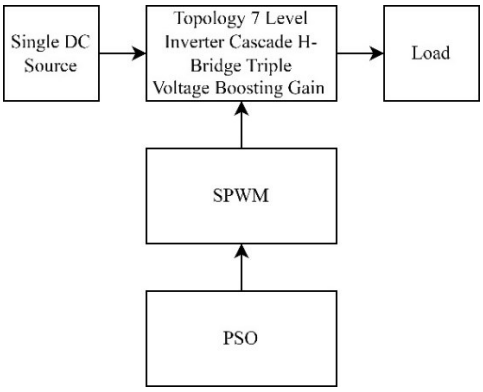

Fig. 4. Block Diagram Research

Table 2. MOSFET Switching Conditions

State	0	+1	+2	+3	-1	-2	-3
S1	0	0	0	0	1	1	1
S2	1	1	1	1	0	0	0
S3	1	1	1	1	1	0	0
S4	0	0	0	0	0	1	1
S5	1	1	1	0	1	0	0
S6	1	1	1	0	1	1	1
S7	0	0	0	1	0	0	0
S8	1	1	1	1	1	1	0
S9	0	0	0	0	0	0	1
S10	1	1	0	0	1	1	0
S11	1	1	0	0	1	1	1
S12	0	0	1	1	0	0	0
S13	0	1	1	1	0	0	0
S14	1	0	0	0	1	1	1

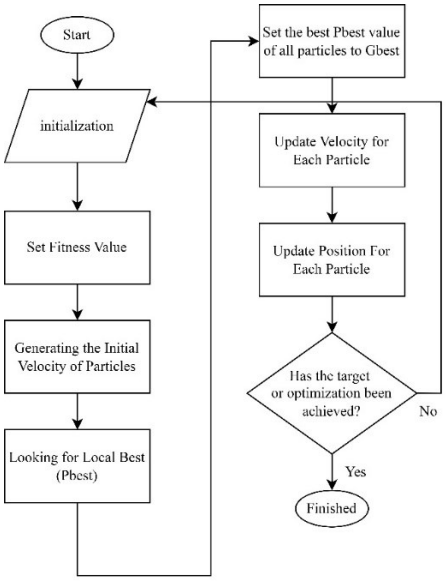

Fig. 5. PSO Flowchart

3. RESULTS AND DISCUSSION

3.1. Modelling Topology

The 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology circuit configuration is depicted in Fig. 6. Consists of three H-bridges. The middle H-bridge is connected to a dc source while the front and rear ends of the H-bridge are each connected to a capacitor. The Cascade H Bridge is connected to a bidirectional voltage blocking switch consisting of two MOSFETs with their Source terminals connected together. To produce higher voltage levels, the switched-capacitor concept is connected in parallel to the dc source. Even though it uses only one DC source, the maximum voltage level is 3VDC, which is an advantage of this topology. The modeling is shown in Fig. 6.

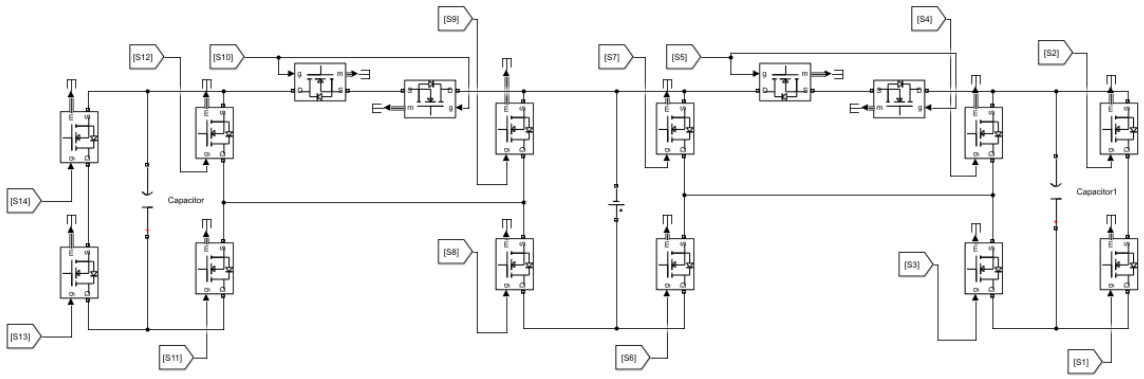

Fig. 6. Modelling Topologi 7 Level Inverter Cascade H- Bridge Triple Voltage Boosting Gain

Fig. 7 illustrates the main waveforms of the 7 Level Inverter Cascade H- Bridge Triple Voltage Boosting Gain topology. The angles for the output voltage levels Vdc, 2Vdc and 3Vdc are defined as θ1, θ2 and θ3 respectively. Capacitor C1 discharges in a shorter time during the positive half cycle (3Vdc) than during the negative half cycle (−2Vdc and −3Vdc). Where the C2 usage period completes the C1 usage period, namely for 2Vdc, 3Vdc and −3Vdc. With a symmetric output voltage and a symmetric load current of more than half the fundamental cycle, the complementary discharge circuit of C1 and C2 can ensure equal changes in electric charge in both capacitors. Therefore, its average voltage is automatically balanced during operation. The voltage ripple on the capacitor can be obtained by considering the longest discharge period, namely from (π + θ2) to (2π − θ2) for C1, and from (θ2) to (π −θ2) for C2. In this case, the capacitor is connected in series with the load. Therefore changes in electric charge depend on the load current and power factor.

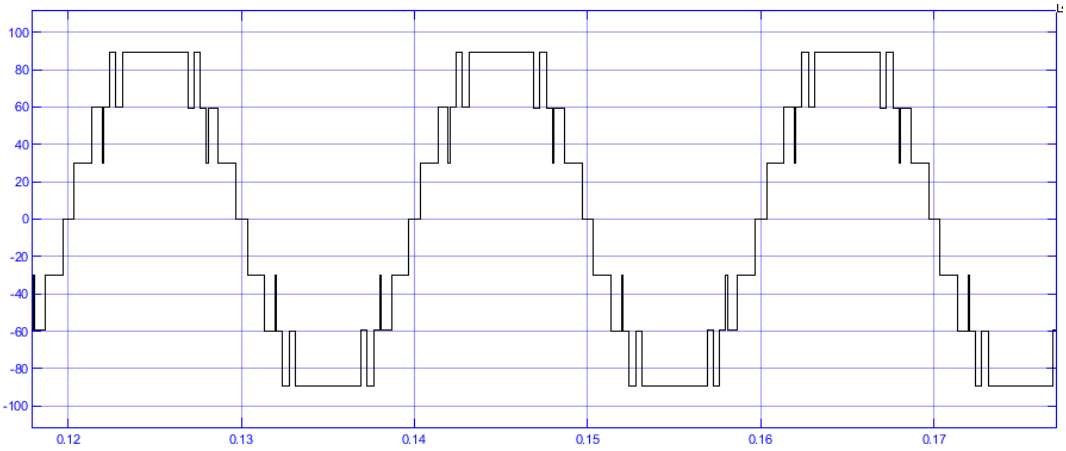

Fig. 7. The output form of the Topologi 7 Level Inverter Cascade H- Bridge Triple Voltage Boosting Gain

The results of the topology simulation with the 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology produce a boosting gain three times the input voltage. The DC voltage input in the topology above is 30 Volts and produces an output voltage value of 90 Volts. A switching scheme of 14 switches is applied to regulate ON/OFF on the MOSFET with a capacitor value of 4700μF ($C2$) and 4700μF ($C2$).

Modeling of the SPWM technique on a 7 Level Inverter Cascade H- Bridge Triple Voltage Boosting Gain topology is shown in Fig. 8. The form of carrier signal generation and modulation signal is shown in Fig. 9 and Fig. 10.

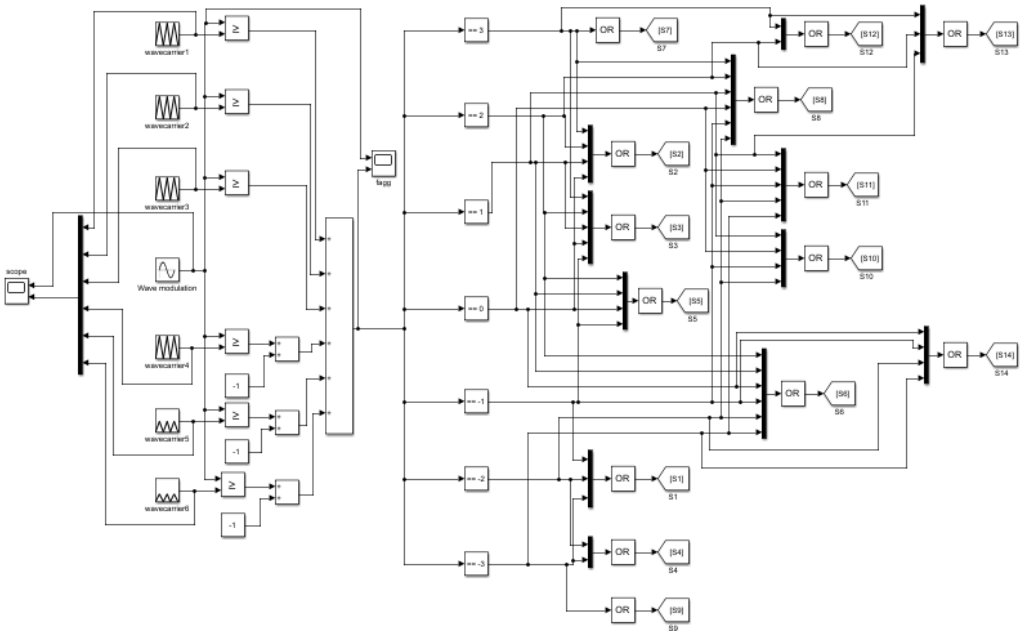

Fig. 8. Modelling SPWM Technique for Topology 7 Level Inverter Cascade H- Bridge Triple Voltage Boosting Gain

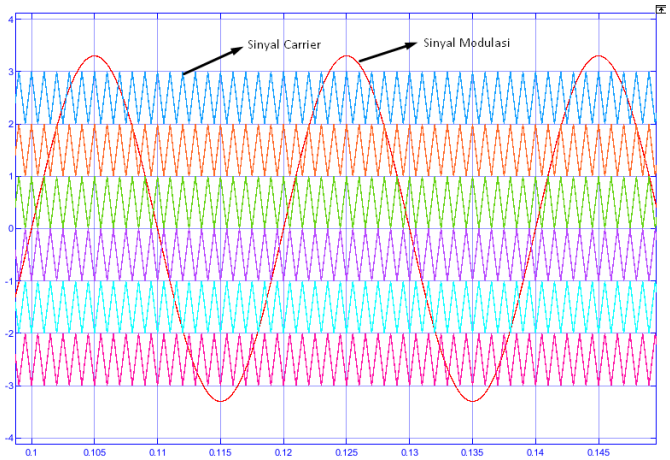

Fig. 9. Input Carrier SPWM Signal

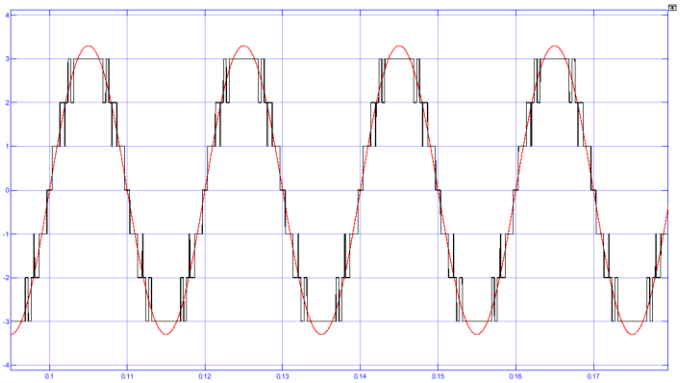

Fig. 10. Output Carrier SPWM Signal

3.2. SPWM Topology 7 Level Inverter Cascade H- Bridge Triple Voltage Boosting Gain

The SPWM modulation technique is used for switching on and off the MOSFET on the inverter by comparing the sinusoidal modulation signal to the carrier signal. By using a 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology with a carrier frequency of 1000 Hz, and a sinusoidal modulation reference signal frequency of 50 Hz. The THD value is shown in Fig. 11.

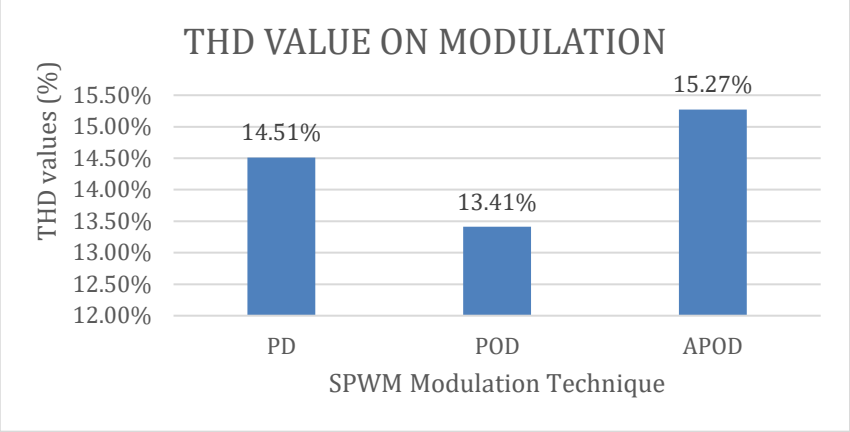

Fig. 11. Comparison of THD Values based on SPWM modulation technique

Based on this data, the PD POD (Fig. 13) and APOD (Fig. 14) modulation techniques have THD values of 14.51%, 13.41%, 15.27% respectively. From these values it can be concluded that the POD technique has the lowest THD value compared to other SPWM techniques so that this technique is then used for SPWM optimization based on the PSO algorithm. THD PD PWM shown in Fig. 12.

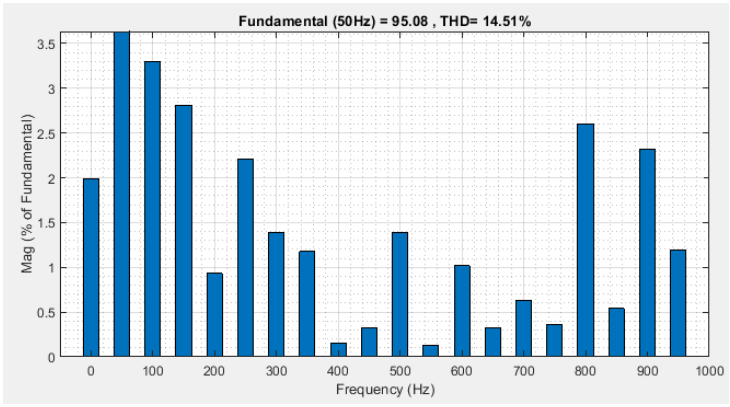

Fig. 12. THD PD PWM

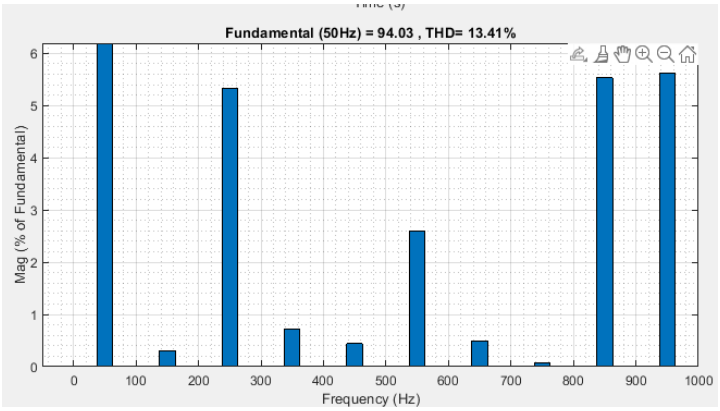

Fig. 13. THD POD PWM

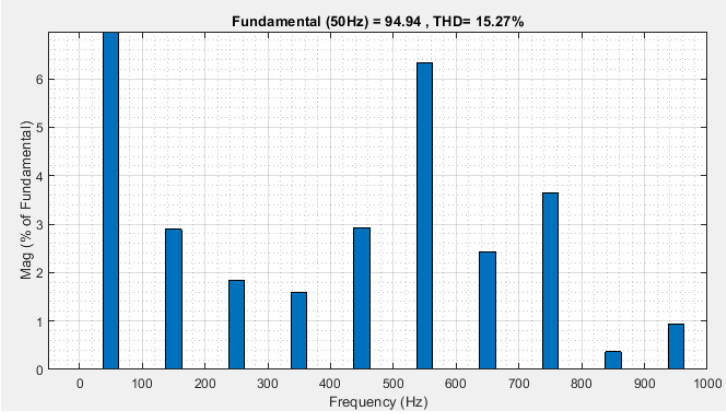

Fig. 14. THD APOD PWM

3.3. Optimization PSO for Topology 7 Level Inverter Cascade H- Bridge Triple Voltage Boosting Gain

Based on simulation results on the 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology with POD modulation techniques, the THD value is 13.41%. The THD value still exceeds the permitted IEEE 519 standard of 8%. Therefore, optimization is carried out on the modulation of the carrier signal regarding time value and frequency in order to be able to reduce the THD so that it does not exceed the permitted standards. PSO optimization value results shown in Table 3.

Table 3. PSO Optimization Value Results

Frequency	A (Start)	B (Max)	C (Start)	Fitness	THD
700	0	0.1000000000	1.4056383045	8.4141912651	8.41
750	0	0.9928380465	1.1000000000	8.9294114706	8.93
800	0	0.2515109835	1.1461520552	8.0489322416	8.05
850	0	1.0000000000	1.1070188426	8.9707601492	8.97
900	**0**	**0.1000000000**	**1.1168529281**	**7.8043596725**	**7.80**
950	0	1.0000000000	1.1047322624	9.0158976748	9.02
1000	0	0.1000000000	1.1047111799	8.2313168111	8.23
1050	0	1.0000000000	1.3091363871	9.3587164162	9.36
1100	0	0.1000000000	1.1062989117	9.0098540141	9.01
1150	0	0.1000000000	1.4428602759	9.3206038956	9.32
1200	0	0.6317553673	1.5000000000	9.4638775811	9.46
1250	0	1.0000000000	1.2655859756	10.183825385	10.18
1300	0	0.1000000000	1.4510292058	9.6473595621	9.65

Carrier signal parameters consisting of Time value and frequency were obtained using the PSO algorithm which was carried out in 20 iterations and generated 150 particles randomly. Optimization of the carrier signal to minimize the THD value at the output of the 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology is carried out until the maximum convergence or iteration value is reached. The results of the optimized parameters for time value and carrier signal are shown in Table 3. In this table it can be seen that the Gbes value of each particle A, B, C and frequency is [0 0.1000000000 1.1168529281]/ 900 with a fitness value of 7.8043596725% has a THD value of 7.80%, and meets IEEE 519 standards. PSO optimization results shown in Fig. 15. THD value based on FFT analyzer shown in Fig. 16. Voltage wave signal in 7 level inverter cascade h- Bridge topology triple voltage boosting gain with PSO optimization shown in Fig. 17.

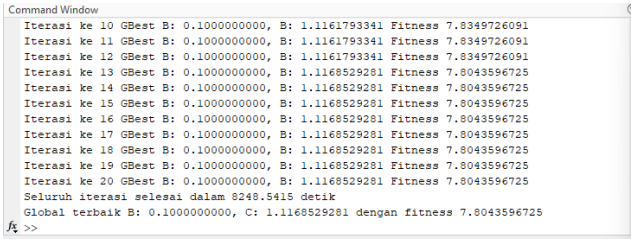

Fig. 15. PSO optimization results

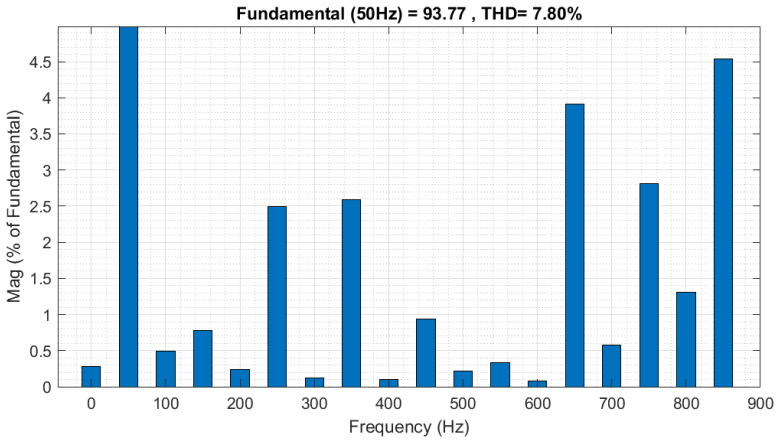

Fig. 16. THD value based on FFT Analyzer

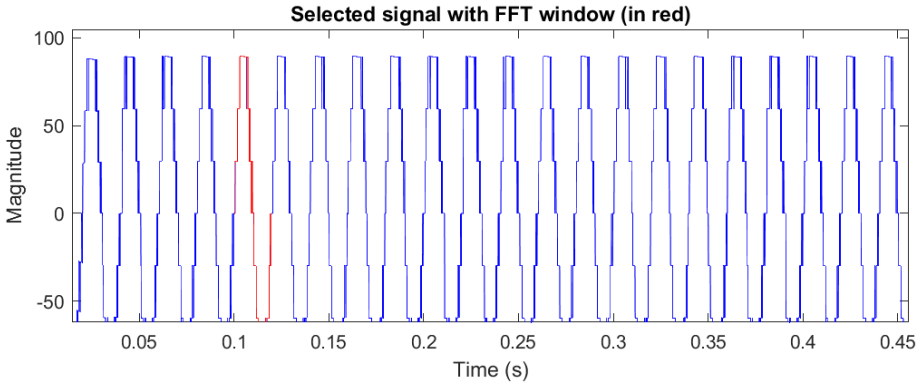

Fig. 17. Voltage wave signal in 7 Level Inverter Cascade H- Bridge Topology Triple Voltage Boosting Gain with PSO optimization

Next, the optimization carried out was compared with the Genetic Algorithm as a comparison with 150 populations that were raised and produced the following values in Table 4. The value obtained from this algorithm is 7.80% for PSO and 8.20% for GA, which shows that the PSO algorithm is better than GA in optimizing the switching topology of the 7 Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain.

In Table 5, a comparison of 7 MLI levels is shown. The use of the PSO optimization algorithm in modifying the carrier signal can reduce THD by up to 7.80% and has the best THD value compared to the others. Where the largest THD value is 21%.

Table 4. Comparison of optimization results of the PSO algorithm and Genetic Algorithm

Frequency	THD PSO	THD GA
700	8.41	9.09
750	8.93	9.11
800	8.05	9.22
850	8.97	9.49
900	**7.80**	8.20
950	9.02	9.57
1000	8.23	8.74
1050	9.36	9.40
1100	9.01	9.52
1150	9.32	9.52
1200	9.46	9.76
1250	10.18	10.44
1300	9.65	10.64

Table 5. Comparison Of THD Values With Previous Research With 7 CHB Levels

Author	Title	THD	THD PSO
Youssef Babkrani [33]	Implementation of a modified carrier-based PWM technique for a cascaded MLI using DSP microcontroller	14.77 %	7.80 %
Dipesh Atkar [23]	Control of seven level cascaded H-Bridge inverter by hybrid SPWM technique	17.5 %	
T. Anand Kumar [45]	Genetic Algorithm Based 7-Level Step-Up Inverter with Reduced Harmonics and Switching Devices	21 %	
Shaji L. [13]	Performance analysis of a new single phase single source 7-level inverter topology using different SPWM techniques	17.27%	

4. CONCLUSION

This research models a 7-level Inverter Cascade H- Bridge Triple Voltage Boosting Gain topology using MATLAB/SIMULINK Software. The results of the topology simulation with the 7-Level Inverter Cascade H-Bridge Triple Voltage Boosting Gain topology produce a boosting gain three times the input voltage. The DC voltage input in the topology above is 30 Volts and produces an output voltage value of 90 Volts. A switching scheme of 14 switches is applied to regulate ON/OFF on the MOSFET with a capacitor value of 4700μF ($C2$) 4700μF ($C2$). The POD-PWM type SPWM technique in the research conducted produced a THD of 13.41% better than the PD-PWM modulation technique of 14.51% and APOD-PWM of 15.27%. With the POD-PWM type SPWM technique, THD was 19.62%. The SPWM technique uses a carrier frequency of 1000 Hz and a sinusoidal modulation reference signal frequency of 50 Hz. The POD – PWM technique which was optimized using the PSO algorithm was carried out in 20 iterations and generated 150 particles randomly. Optimization of the carrier signal frequency parameter of 900 Hz produces a THDv and THDi value of 7.80% with a time value of [0 0, 0.1000000000 1.1168529281]/900. The THDv optimization value was compared with another optimization algorithm, namely the Genetic Algorithm, with the smallest THDv value of 8.20%. The THDv value from the PSO optimization is stated to be in accordance with the IEEE 519 standard with a maximum permitted THDv of 8% and this value is better than previous research, namely 17.27%.

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